AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please replace the paragraph starting on page 10, line 9 with the following paragraph:

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a representation of an optical disc;

FIG. 2 illustrates, in some detail, a structure of the optical disc of FIG. 1 and a relationship between tracks on the disc and photodiodes designed to recover reflected laser light;

FIG. 3 illustrates a relationship between a push-pull signal and a recovered clock;

FIG. 4 is a perspective view of tracks exhibiting wobble in a DVD-RAM;

FIG. 5 is a block diagram of wobble signal generation circuitry according to a preferred embodiment of the present invention;

Fig. 6 is a timing diagram illustrating a relationship between a push-pull signal and a wobble signal obtained therefrom;

FIG. 7 is a block diagram of a header slicer circuit according to a preferred embodiment of the present invention;

FIG. 8 is illustrative of a preferred header detection mechanism of the present invention;

FIG. 9 is a header detect logic state machine flow diagram according to the present invention; ~~and~~

FIG. 10 is a flow diagram of a preferred operating methodology employed by the present invention in acquiring phase lock; and

FIG. 11 is a diagram of an alternative embodiment of the invention.

Please replace the paragraph starting on page 24, line 4 with the following paragraph:

Referring to FIG. 11, alternative ~~Alternative~~ embodiments of the invention may be implemented as computer program code 430 encoded on a computer program or readable medium 432 for use with a computer system 434. It is expected that such a computer program product may be distributed as a removable medium with accompanying printed or electronic documentation, preloaded with ~~a~~ the computer system 434 or distributed from a server or electronic bulletin board over a network (e.g., the Internet or World Wide Web). A series of computer instructions can be fixed either on a tangible medium or in a computer data signal embodied in a carrier wave, transmittable to ~~a~~ the computer system 434 using wireline or

wireless transmission techniques. Removable (e.g., tangible) medium may be a computer readable media 432, such as a diskette, CD-ROM, DVD-ROM or RAM, fixed disc, magneto-optical discs, ROMs, flash memory, magnetic or optical cards etc. The series of computer instructions embodies all or part of the functionality previously described herein with respect to the system.

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 16-19 without prejudice. Please add new claims 20-28.

1. (CURRENTLY AMENDED) A method of synchronizing a phase lock loop to an intermittent clock signal, the method comprising the steps of:

(A) seeking to acquire phase lock of the phase lock loop with the intermittent clock signal during a plurality of first periods of the intermittent clock signal when the intermittent clock signal is present;

(B) timing a duration for each of the first periods; and

~~(B)~~ (C) holding the phase lock loop in a free-running state during a plurality of second periods when the intermittent clock signal is absent in response to the duration indicating an end to one of the first periods.

2. (CURRENTLY AMENDED) The method according to claim 1, further comprising the ~~steps~~ step of:

~~(C)~~ acquiring frequency lock in an asynchronous mode.

3. (ORIGINAL) The method according to claim 1, wherein the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc and the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity.

4. (CURRENTLY AMENDED) The method according to claim ~~3, further comprising~~ 1, wherein step (C) comprises the sub-step of:

~~timing a duration of the intermittent clock signal; and~~

placing the phase lock loop in the free-running state in ~~anticipation~~ advance of reading ~~an arrival of~~ a header region on an optical disk in response to ~~an elapsed~~ the duration ~~of the intermittent clock signal~~.

5. (ORIGINAL) The method according to claim 4, further comprising:

identifying re-emergence of the intermittent clock signal; and

seeking to acquire phase lock only after re-emergence of the intermittent clock signal has been validated.

6. (CURRENTLY AMENDED) ~~The method according to claim 3, further~~ A method of synchronizing a phase lock loop to an intermittent clock signal, the method comprising the steps of:

(A) seeking to acquire phase lock during periods of the intermittent clock signal;

(B) holding the phase lock loop in a free-running state during periods when the intermittent clock signal is absent; and

(C) estimating a signal envelope for the intermittent clock signal~~;~~

~~bandpass filtering the header region to generate a spike indicative of a header transition;~~

~~amplifying the signal envelope and the spike to scale the spike relative to the signal envelope to differentiate the signal envelope from the spike;~~

~~defining a threshold exceeding the signal envelope; and~~

~~identifying commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region~~.

7. (CURRENTLY AMENDED) The method according to claim ~~6~~ 20, further comprising the step of:

identifying a relative signal level polarity between a first spike of the spikes and a successive spike of the spikes to identify a requirement for a phase reversal.

8. (ORIGINAL) The method according to claim 6, further comprising:

filtering the intermittent clock signal in a low pass filter to generate an adaptive slice level signal capable of tracking residual near-DC variations in the intermittent clock signal.

9. (CURRENTLY AMENDED) A computer readable medium for use in a computer to synchronize a phase lock loop to an intermittent clock signal, the computer readable medium recording a computer program that is readable and executable by the computer, the computer program configured to execute the steps of ~~claim 1~~:

(A) seeking to acquire phase lock of the phase lock loop with the intermittent clock signal during a plurality of first periods of the intermittent clock signal when the intermittent clock signal is present;

(B) timing a duration for each of the first periods; and

(C) holding the phase lock loop in a free-running state during a plurality of second periods when the intermittent clock signal is absent in response to the duration indicating an end to one of the first periods.

10. (CURRENTLY AMENDED) A system comprising:

~~a control circuit coupled to~~ a phase lock loop arranged to receive an intermittent clock signal to which the phase lock loop is to be synchronized~~, the~~; and

a control circuit configured to (i) maintain ~~operation~~ operational control of the phase lock loop, (ii) determine a plurality of first periods of time when the intermittent ~~clocking~~ clock signal is stable, (iii) selectively maintain the phase lock loop in a phase acquisition state during ~~said~~ the first periods of time, and (iv) force the phase lock loop to enter a free-running state during a plurality of second periods of time when the intermittent clock signal is absent ~~or not stable~~.

11. (CURRENTLY AMENDED) The ~~control circuit~~ system of claim_10, wherein the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc and the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity and which each define a data sector, the control circuit ~~further~~ comprising:

a counter arranged to time the intermittent clock signal during each of the data sectors ~~sector~~, wherein the control circuit is further configured to force the phase lock loop to enter ~~a~~ the free-running state ~~being operationally~~ in response to the time ~~elapsed~~ within each of the data sectors ~~sector and the phase lock~~

~~loop is placed in the free-running state, based on time elapsed,~~ and in advance of an arrival of ~~a~~ each of the header regions.

12. (CURRENTLY AMENDED) ~~The control circuit of claim 11, further~~ A system comprising:

a phase lock loop arranged to receive an intermittent clock signal to which the phase lock loop is to be synchronized;

a control circuit configured to (i) maintain operational control of the phase lock loop and (ii) force the phase lock loop to enter a free-running state during periods of time when the intermittent clock signal is not stable; and

a detector arranged to identify emergence of a steady state in the intermittent clock signal, wherein the control circuit is further configured to force the phase lock loop to enter ~~the free-running~~ an acquisition state~~, being operationally disabled by the detector,~~ in response to the steady state.

13. (CURRENTLY AMENDED) ~~The control circuit of claim 11, further~~ A system comprising:

a phase lock loop arranged to receive an intermittent clock signal to which the phase lock loop is to be synchronized;

a control circuit configured to (i) maintain operational control of the phase lock loop, (ii) determine periods of time when the intermittent clocking signal is stable, (iii) selectively

maintain the phase lock loop in a phase acquisition state during the periods of time and (iv) force the phase lock loop to enter a free-running state during periods of time when the intermittent clock signal is absent; and

~~a top hold feedback circuit arranged to estimate a signal envelope for the intermittent clock signal;~~

a bandpass filter configured to ~~receive the intermittent clock~~ filter an input signal~~, the bandpass filter arranged to filter the header region~~ to generate the intermittent clock signal and a plurality of spikes ~~spike~~ indicative of a header region of an optical disk ~~transition;~~

~~an amplifier configuration arranged to amplify the signal envelope and the spike, to scale the spike relative to the signal envelope to differentiate the signal envelope from the spike;~~

~~a data slicing circuit configured to define a threshold exceeding the signal envelope; and~~

~~a comparator arrangement arranged to identify commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region~~.

14. (CURRENTLY AMENDED) The ~~control circuit~~ system of claim ~~13~~ 27, wherein the comparator arrangement comprises a first and a second comparators configured to process opposite signal

senses from the signal envelope, the first and the second comparators each providing an output to a controller arranged to identify ~~the~~ a relative signal level polarity between ~~a~~ the first spike and a successive spike of the spikes to identify a requirement for a phase reversal in the phase lock loop.

15. (CURRENTLY AMENDED) The ~~control circuit~~ system of claim 12, further comprising:

a low pass filter arranged to generate an adaptive slice level signal capable of tracking residual DC variations in the intermittent clock signal in response to a filtered clock signal.

16. (CANCELED)

17. (CANCELED)

18. (CANCELED)

19. (CANCELED)

20. (NEW) The method according to claim 6, further comprising the step of:

bandpass filtering an input signal to generate a plurality of spikes indicative of a transition for a header region on an optical disk.

21. (NEW) The method according to claim 20, further comprising the step of:

amplifying the signal envelope and the spikes to scale the spikes relative to the signal envelope to differentiate the signal envelope from the spikes.

22. (NEW) The method according to claim 21, further comprising the step of:

defining a threshold exceeding the signal envelope.

23. (NEW) The method according to claim 22, further comprising the step of:

identifying commencement of the header region by equating a first transition of the spikes through the threshold as being indicative of the header region.

24. (NEW) The system of claim 13, further comprising:

a top hold feedback circuit arranged to estimate a signal envelope for the intermittent clock signal.

25. (NEW) The system of claim 24, further comprising:

an amplifier configured to amplify the signal envelope and the spikes, to scale the spikes relative to the signal envelope to differentiate the signal envelope from the spikes.

26. (NEW) The system of claim 24, further comprising:

a data slicing circuit configured to define a threshold exceeding the signal envelope.

27. (NEW) The system of claim 26, further comprising:

a comparator arrangement configured to identify commencement of the header region by equating a first spike of the spikes transitioning through the threshold as being indicative of the header region.

28. (NEW) The system of claim 13, further comprising:

an array of photodiodes adapted to recover an input signal representation from an optical disc containing data segments interspersed with the header regions.

AMENDMENTS TO THE DRAWINGS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

A new FIG. 11 has been added to illustrate the computer system and the program code within the computer readable medium as discussed on page 24, lines 4-15 of the specification and claim 9. Approval of the new figure is respectfully requested.